CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS IN THE CLAIMS

1. (Currently Amended) A method for pre-configuring an FPGA to a known state during a reset condition or prior to the FPGA undergoing system initialization, the method comprising:

loading a configuration value for an on-chip device of the FPGA into a flip-flop interconnected to said on-chip device; and

transferring said configuration value from said flip-flop to said on-chip device, said transfer of said configuration value effectuating pre-configuration of said on-chip device;

wherein said flip-flop is a D-type flip-flop.

2. (Original) The method according to claim 1, further comprising pre-storing said configuration value in a memory cell of the FPGA.

3. (Original) The method according to claim 2, wherein said memory cell is a BRAM.

4. (Original) The method according to claim 2, further comprising transferring said configuration value from said memory cell to said flip-flop upon power-up of the FPGA.

5. (Original) The method according to claim 4, further comprising the supplying a clock signal to said flip-flop to effectuate said transfer of said configuration value from said memory cell to said flip-flop upon power-up of the FPGA.

6. (Original) The method according to claim 1, further comprising supplying a clock signal to said flip-flop to effectuate said transfer of said configuration value from said flip-flop to said on-chip device.

7. (Canceled)

8. (Original) The method according to claim 1, wherein said flip-flop is a configuration register for said on-chip device.

9. (Original) The method according to claim 1, wherein said on-chip device is an on-chip memory controller.

10. (Currently Amended) A method for pre-configuring an FPGA during a reset condition or prior to system initialization of the FPGA, the method comprising:

loading a value into at least one flip-flop of the FPGA, said at least one flip-flop functioning as a configuration register for an on-chip device of the FPGA; and

configuring said FPGA on-chip device to a particular state using said loaded value from said at least one flip-flop;

wherein said value is a bit.

11. (Currently Amended) The method according to claim 10, wherein said loading step further comprises:

transferring said ~~at least one~~ value stored in at least one memory cell of the FPGA to said flip-flop; and

storing said transferred ~~at least one~~ value in said at least one flip-flop of the FPGA.

12. (Currently Amended) The method according to claim 11, wherein said loading step further comprises the step of loading said transferred ~~at least one~~ value into said at least one flip-flop whenever the FPGA is powered up.

13. (Original) The method according to claim 11, wherein the step of transferring further comprises storing said value for configuring said FPGA on-chip device in said at least one memory cell, said stored value representing a default state of said memory cell.

14. (Canceled)

15. (Currently Amended) A system for pre-configuring an FPGA to a known state during a reset condition or prior to the FPGA undergoing system initialization, the system comprising:

a flip-flop coupled to an on-chip device of the FPGA; and

a clock transitioning circuit coupled to said flip-flop for causing,

a configuration value for said FPGA on-chip device to be loaded into said flip-flop; and

said configuration value to be read by said on-chip device, said reading of said configuration value effectuating the pre-configuration of said on-chip device;

wherein said flip-flop is a D-type flip-flop.

16. (Original) The system according to claim 15, further comprising an FPGA memory cell for pre-storing said configuration value.

17. (Original) The system according to claim 16, wherein said memory cell is a BRAM.

18. (Canceled)

19. (Original) The system according to claim 15, wherein said flip-flop is a configuration register for said on-chip device.

20. (Original) The system according to claim 15, wherein said on-chip device is an on-chip memory controller.